AMENDMENTS TO THE CLAIMS

1. (Original) A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced;

a WBL binarization circuit for smoothing edges of a wobble binary signal that is read by the pickup;

a FEP (Front End Processor) for performing band limitation and gain control to a wobble signal that is read by the pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from the FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data on the basis of the digital signal outputted from the ADC;

a waveform shaping circuit for generating a wobble binary signal waveform on the basis of a RF signal that is read by the pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from the WBL binarization circuit with referring to the waveform generated by the waveform shaping circuit; and

a PLL (Phase Locked Loop) circuit that is connected to the phase control circuit, for generating a sync clock on the basis of the phase controlled data,

said address detection circuit and said waveform shaping circuit being digitally configured.

2. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein

the waveform shaping circuit includes a BPF (Band Pass Filter) as a digital filter, and

said digital filter is constituted by an IIR (Infinity Impulse Response) digital filter having a reset function of initializing the digital filter when the digital filter characteristics are divergent.

3. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein

the address detection circuit includes a LPF (Low Pass Filter) as a digital filter, and

said digital filter is constituted by an IIR digital filter having a reset function of initializing the digital filter when the digital filter characteristics are divergent.

4. (Currently Amended) The wobble signal processing apparatus as defined in Claim 2 ~~or 3~~ wherein

the digital filter calculates an optimum tap coefficient value, stores the optimum tap coefficient value in a storage unit that is externally provided, and performs following filtering utilizing the optimum tap coefficient value stored in the storage unit.

5. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein

the address detection circuit comprises:

a digital filter for filtering the output from the ADC; and

a PRML (Partial Response Maximum Likelihood) circuit for correcting errors in the signal outputted from the digital filter, and detecting the ADIP signal using the corrected signal.

6. (Original) The wobble signal processing apparatus as defined in Claim 5 wherein

a PRML system that is implemented by the PRML circuit is a PR(a,b) system.

7. (Original) The wobble signal processing apparatus as defined in Claim 6 wherein

parameter values in the PR(a,b) system have a relationship of a=b.

8. (Original) The wobble signal processing apparatus as defined in Claim 5 wherein

the PRML circuit switches a sampling method between a peak sampling method and an offset sampling method.

9. (Original) The wobble signal processing apparatus as defined in Claim 8 wherein

the PRML circuit performs the sampling in a cycle of 8T.

10. (Original) The wobble signal processing apparatus as defined in Claim 5 wherein

the PRML circuit performs a standardized Euclidean distance algorithm in a computing circuit of a Viterbi decoder by the PRML system.

11. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein

the address detection circuit comprises:

a first digital filter for filtering the output from the ADC;

a phase control circuit for controlling the phase of the wobble binary signal outputted from the WBL binarization circuit with referring to the signal outputted from the first digital filter, and outputting a phase controlled signal;

a multiplier for multiplying the signal outputted from the first digital filter by the phase controlled signal;

a second digital filter for filtering an output from the multiplier;

an edge smoothing circuit for binarizing the signal outputted from the first digital filter, and smoothing edges of the binarized signal, thereby generating a clock for outputting the ADIP signal; and

a binarization circuit for binarizing the signal outputted from the second digital filter in accordance with the clock that is outputted from the edge smoothing circuit, and outputting the ADIP signal.

12. (Currently Amended) The wobble signal processing apparatus as defined in Claim 1 ~~or 11~~ wherein

the phase control circuit obtains a phase difference between the wobble binary signal and the wobble signal that has passed through the digital filter, and controls the phase by delaying the wobble binary signal.

13. (Original) The wobble signal processing apparatus as defined in Claim 12 wherein the phase control circuit corrects a phase shift by performing counter processing to clock delay information previously obtained.

14. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein the address detection circuit comprises:

a digital filter for filtering the output from the ADC; and

a DSV (Digital Sum Value) calculator for digitally processing the output from the digital filter by dividing the same with a predetermined threshold value, thereby detecting the ADIP signal.

15. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein the address detection circuit comprises:

a digital filter for filtering the output from the ADC;

a binarization circuit for binarizing the output from the digital filter; and

a counter circuit for counting the number of +1 and the number -1 in the signal outputted from the binarization circuit, and

the ADIP signal is detected on the basis of the count values of the counter circuit.

16. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein the ADC has a 7-bit resolution.

17. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein the FEP further includes an AGC (Auto Gain Control) circuit for performing automatic amplitude control when the amplitude of the ADIP section is decreased or increased due to crosstalk in the optical disc medium.

18. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein

the pickup further includes an aperture ratio decision unit for deciding the degree of distortion of the waveform that is read from the optical disc medium, and controls the diameter of a beam spot of a pickup laser on the basis of the decided degree of distortion of the waveform, thereby controlling the degree of signal component extraction.

19. (Original) The wobble signal processing apparatus as defined in Claim 1 wherein

said apparatus operates in accordance with the sync clock that is supplied from the PLL circuit, and

the sync clock is adaptively changed according to an angular velocity of the disc.

20. (New) The wobble signal processing apparatus as defined in Claim 3 wherein

the digital filter calculates an optimum tap coefficient value, stores the optimum tap coefficient value in a storage unit that is externally provided, and performs following filtering utilizing the optimum tap coefficient value stored in the storage unit.

21. (New) The wobble signal processing apparatus as defined in Claim 11 wherein

the phase control circuit obtains a phase difference between the wobble binary signal and the wobble signal that has passed through the digital filter, and controls the phase by delaying the wobble binary signal.

22. (New) The wobble signal processing apparatus as defined in Claim 21 wherein

the phase control circuit corrects a phase shift by performing counter processing to clock delay information previously obtained.